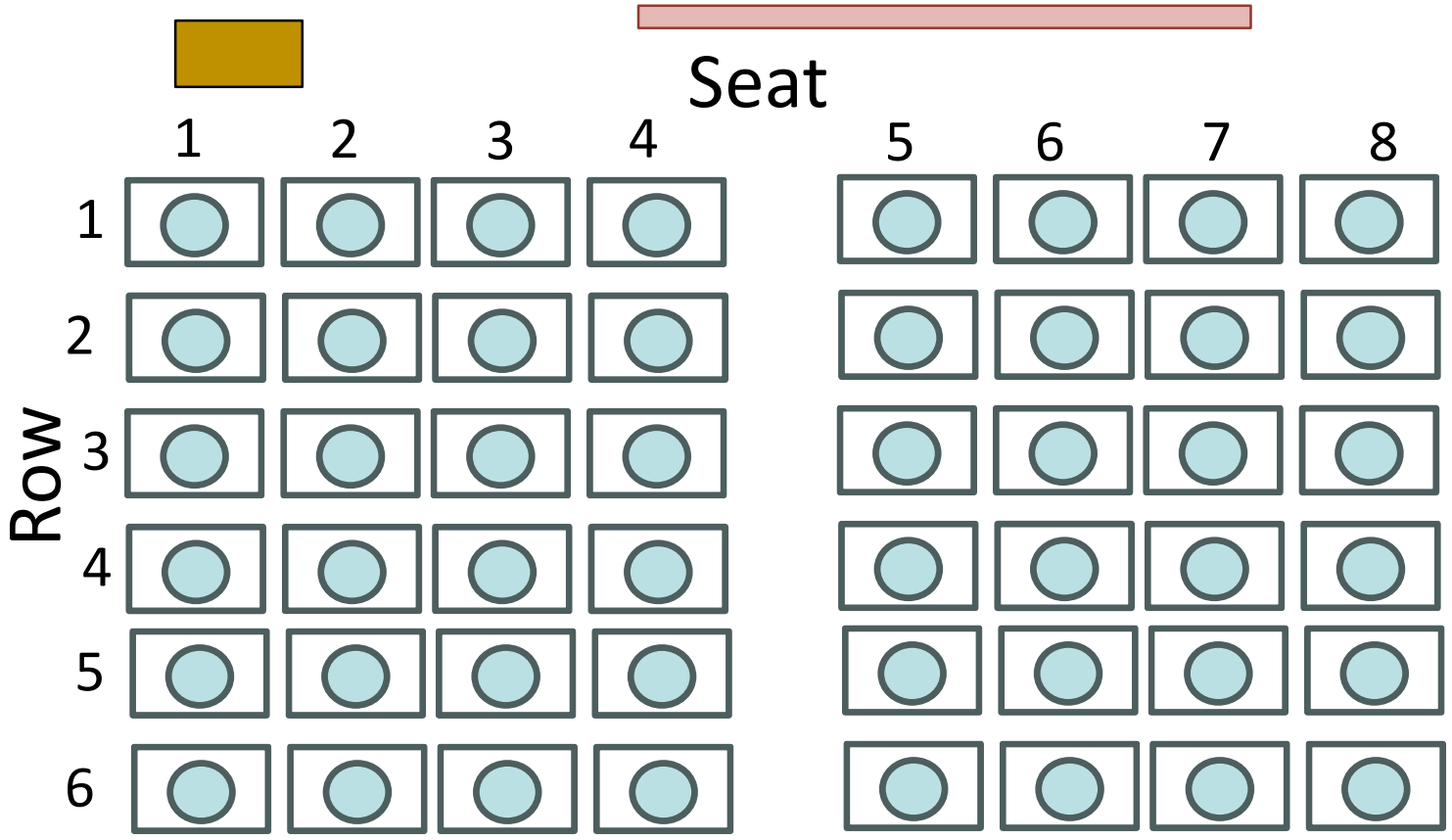
EE 330
Lecture 2

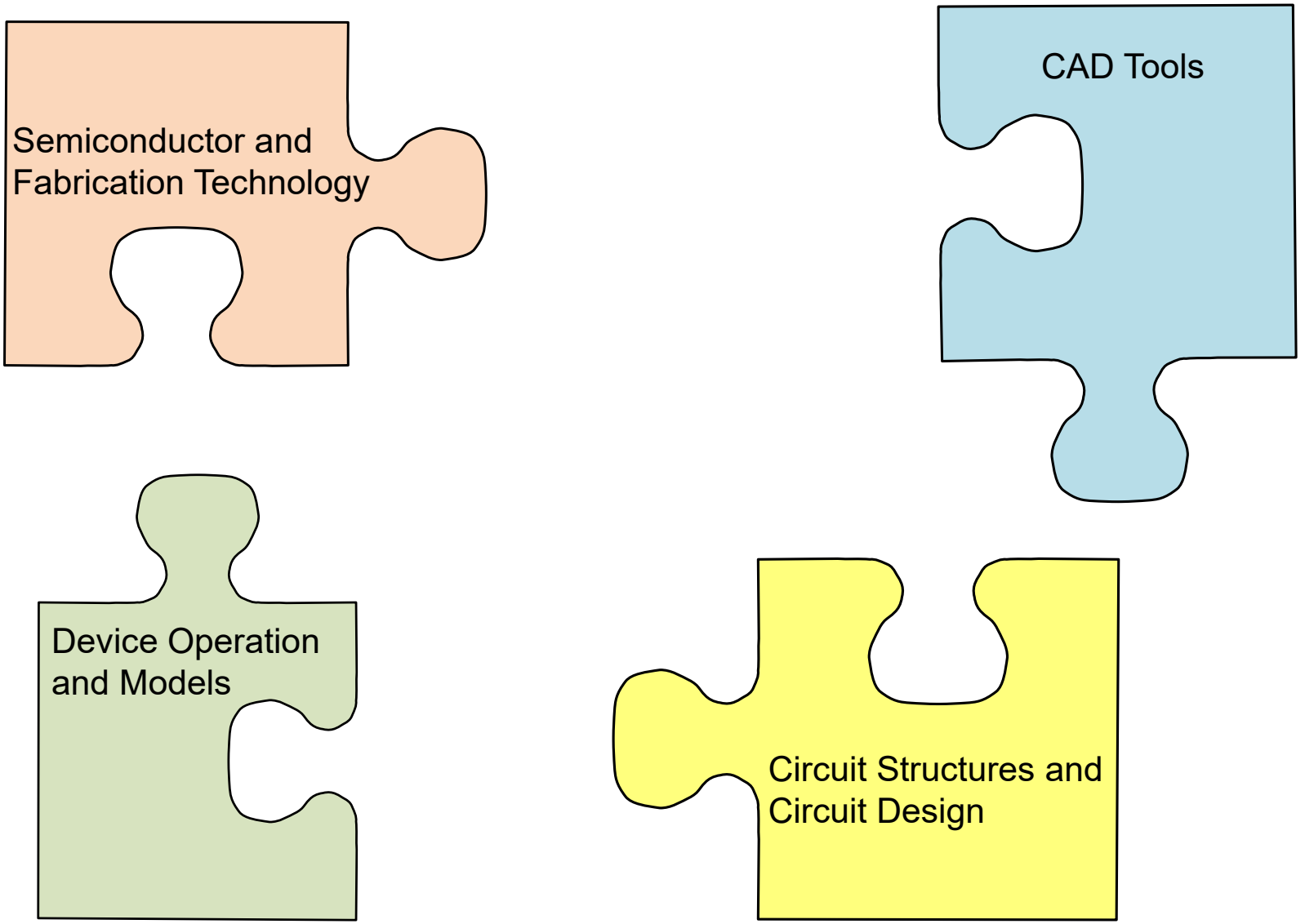
Basic Concepts

Select a seat that will be used for taking attendance.



Review from last lecture:

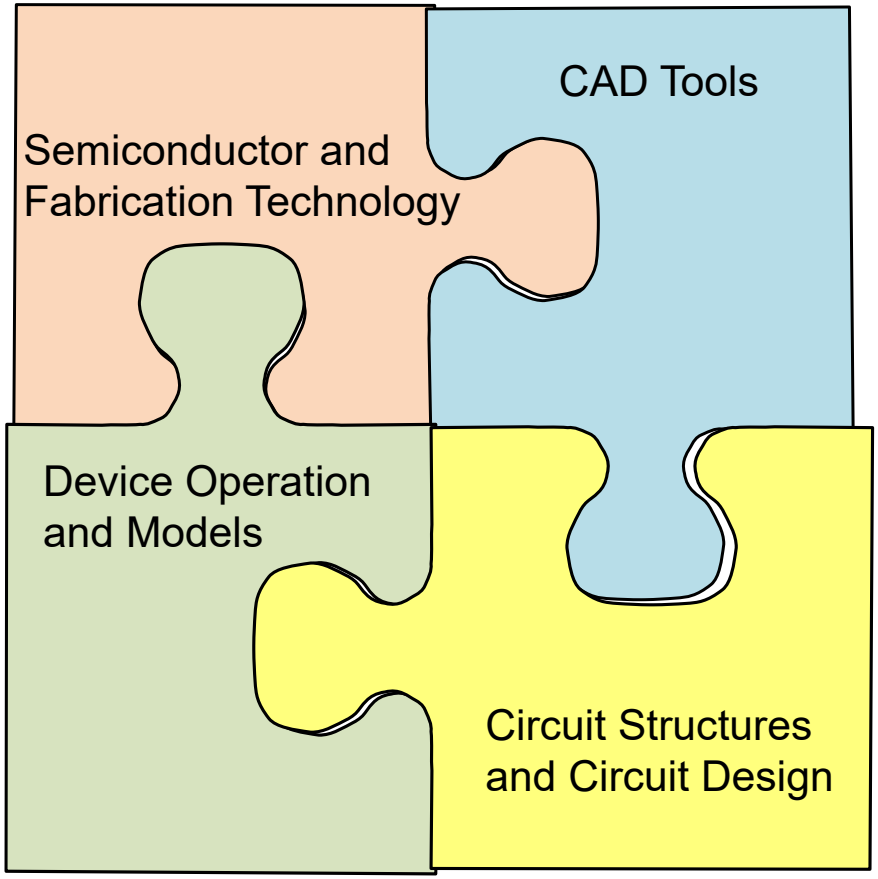
How Integrated Electronics will be Approached



Review from last lecture:

How Integrated Electronics will be Approached

After about four weeks, through laboratory experiments and lectures, the concepts should come together

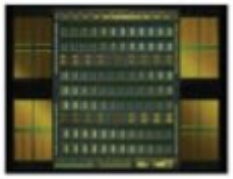


Selected Semiconductor Trends

- AI Chips
- Microprocessors
- DRAMS
- FPGA

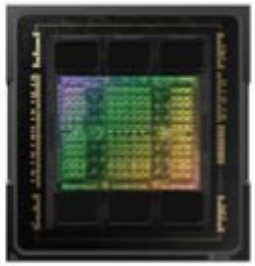
AI Chips

(from Nvidia)

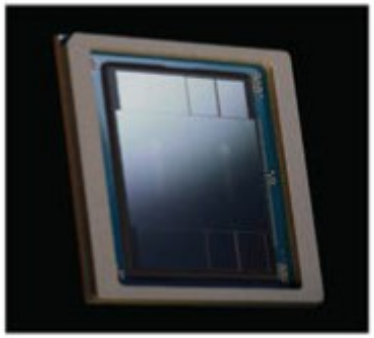


Volta
>21 billion transistors
815mm^2
TSMC 12nm FFN

Ampere
>54 billion transistors
826 mm^2
TSMC N7



Hopper
>80 billion transistors
814 mm^2
TSMC 4N



Blackwell
>208 billion transistors
>1600 mm^2
TSMC 4NP

A New Class of AI Superchip

NVIDIA Blackwell-architecture GPUs pack 208 billion transistors and are manufactured using a custom-built TSMC 4NP process. All NVIDIA Blackwell products feature two reticle-limited dies connected by a 10 terabytes per second (TB/s) chip-to-chip interconnect in a unified single GPU.

Spec Breakout: Key Comparison CPUs

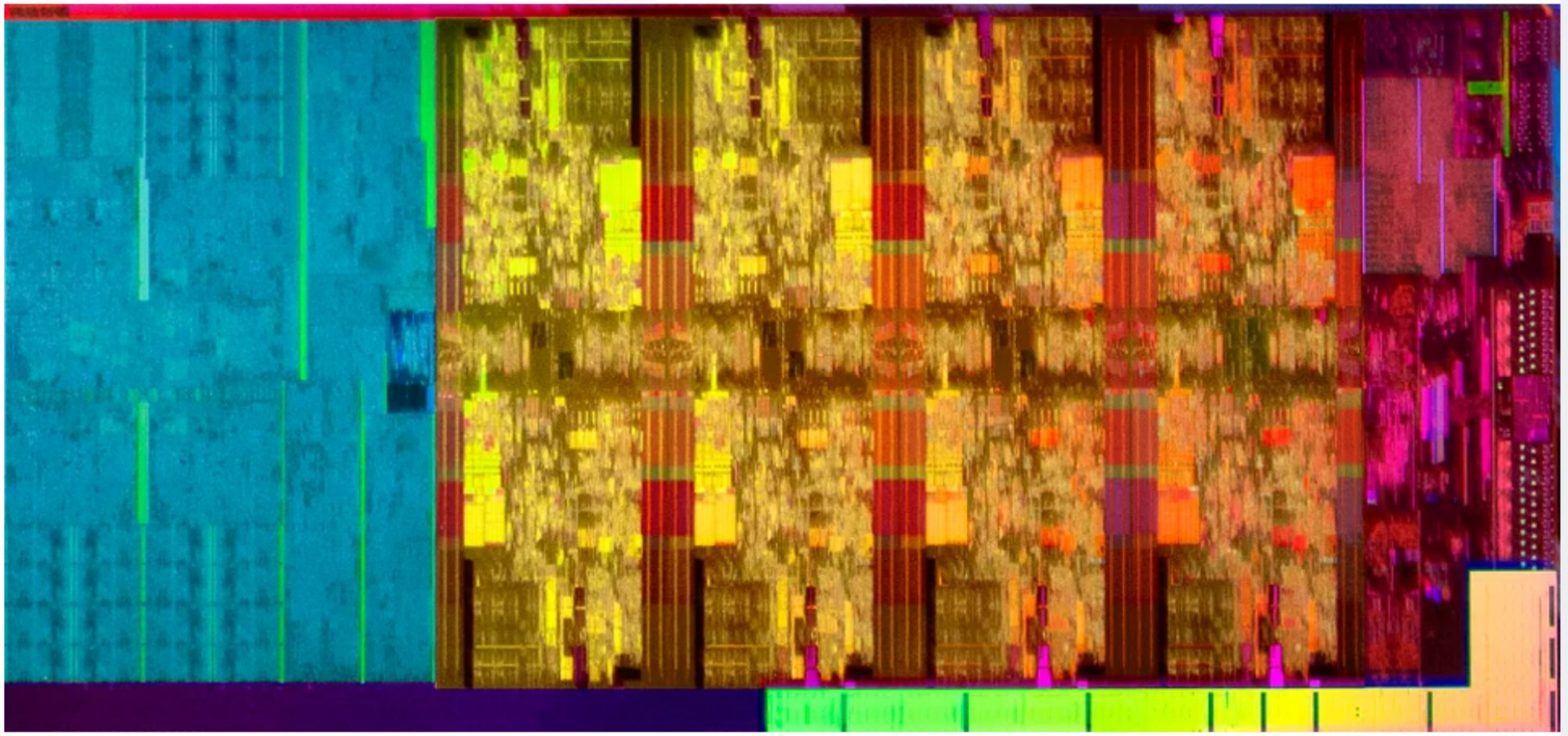
	AMD Ryzen 9 3900X	Intel Core i9-10900K
List Price	$499	$488
Cores	12	10
Threads Supported	24	20
Base Clock	3.8GHz	3.7GHz
Boost Clock	4.6GHz	5.3GHz
Integrated Graphics	None	Intel UHD 630
TDP Rating	105 watts	125 watts
Socket	AM4	LGA1200

AMD Ryzen 9 3900X (64-bit, SIMD, caches, I/O die)	9,890,000,000[1][2]	2019	AMD	7 & 12 nm (TSMC)	273 mm^2

Intel Core i9 10900K 14nm CMOS (between 11B and 26B transistors
Intel 7 process but probably 10nm)

AMD Ryzen 9 now in 4nm node with 20B transistors

Recent Intel Processor

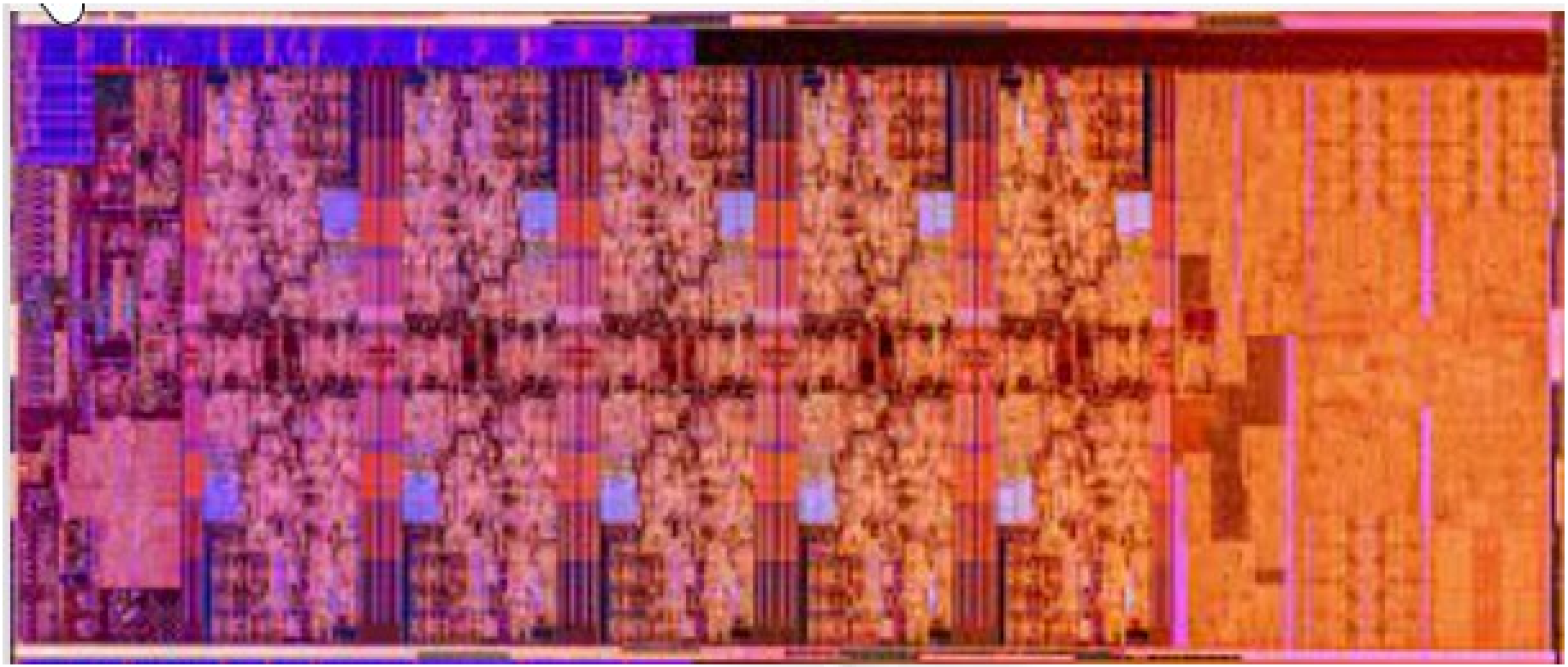


Processor

8 cores, Intel® Core i9 Processor, 5.0 GHz

Power Dissipation: 125 watts

Today!

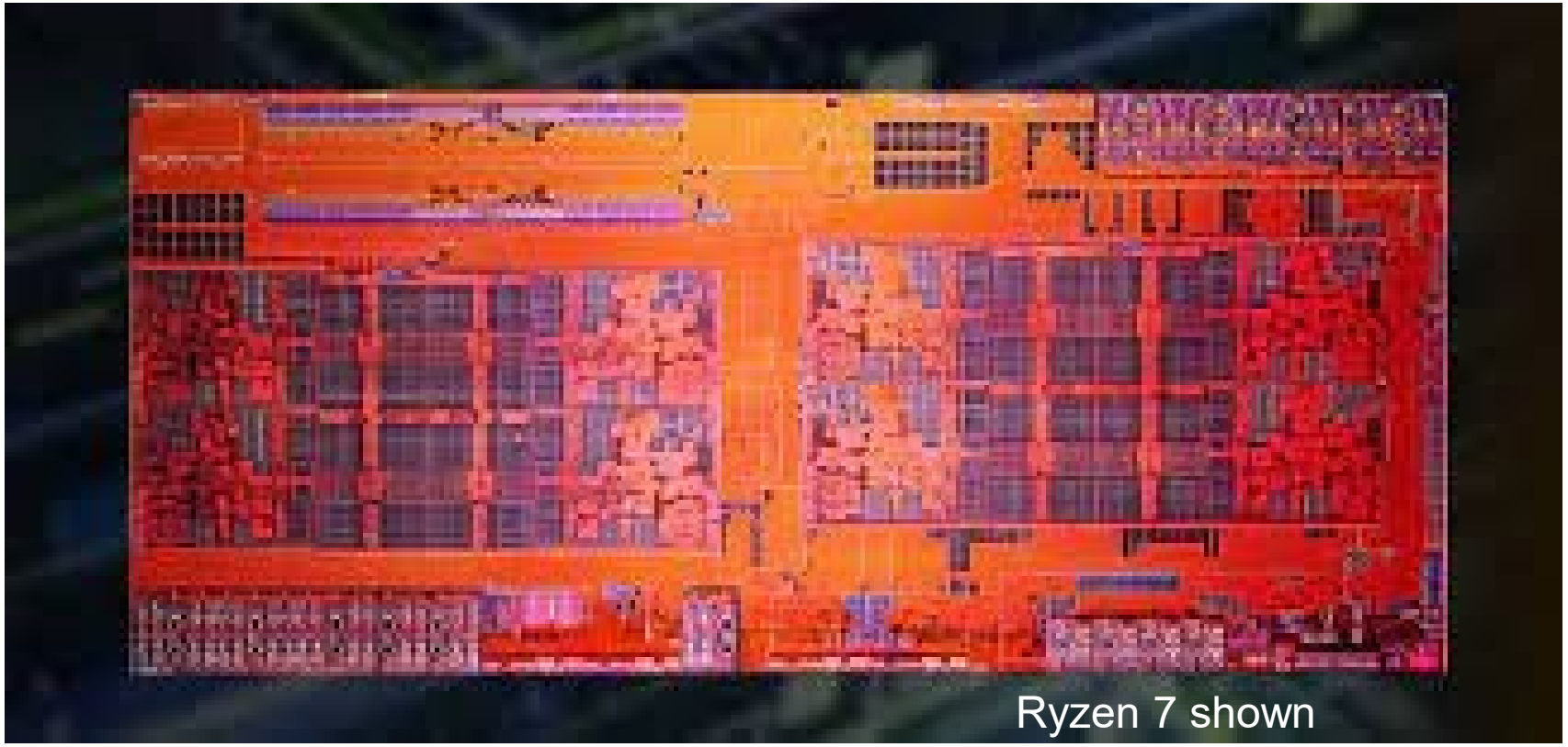


Processor Intel Core i9 10900K

10-core Processor in 14nm CMOS, 3.7GHz

Power Dissipation: 125 watts

Today!

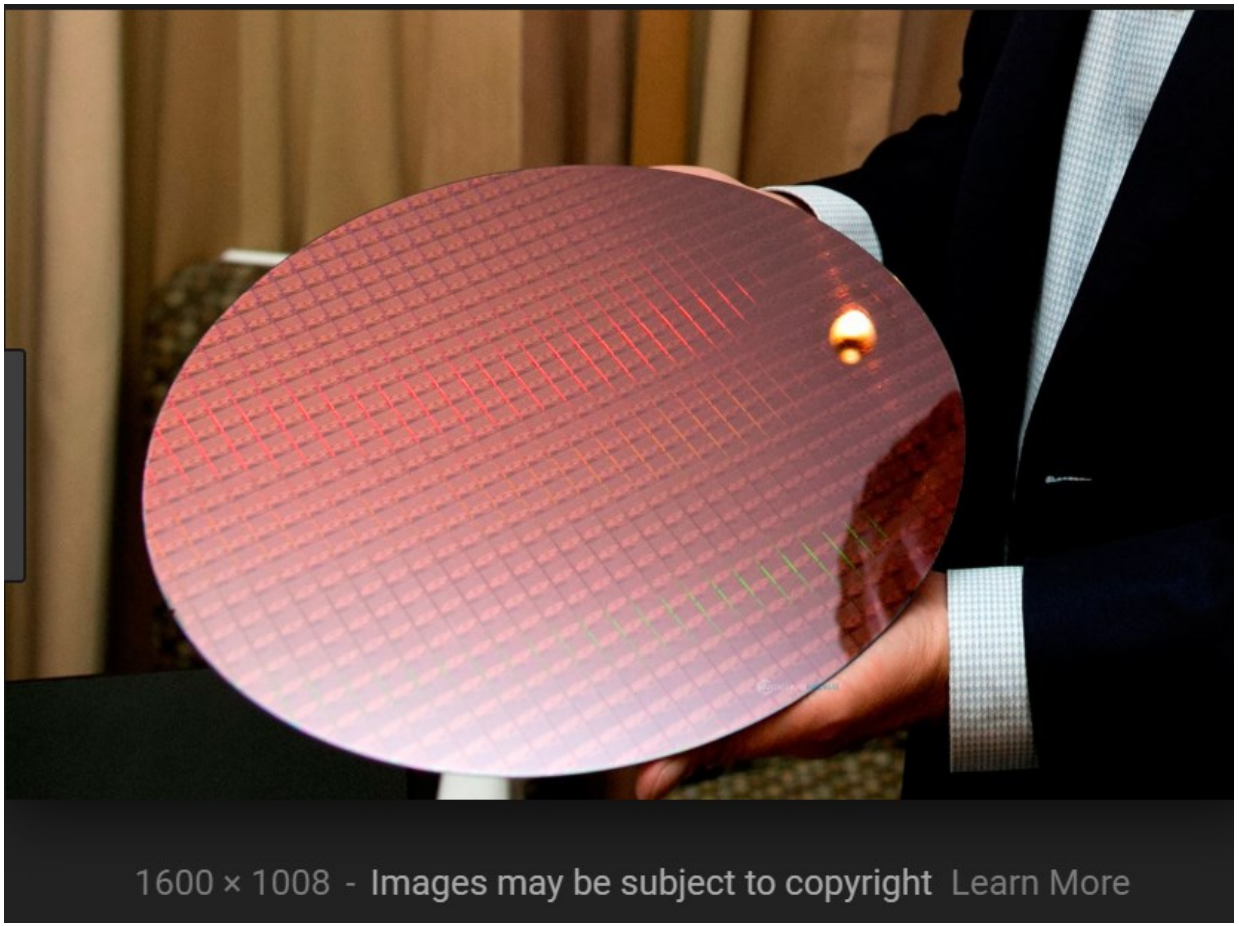


Processor AMD Ryzen 5950X

16-core Processor in 7nm CMOS, 3.4-4.9 GHz

Power Dissipation: 105 watts

Wafer of processors



Yesterday!

Processors

Processor	MOS transistor count	Date of introduction	Designer	MOS process (nm)	Area (mm^2)
MP944 (20-bit, 6-chip, 28 chips total)	74,442 (5,360 excl. ROM & RAM)[24][25]	1970[22][a]	Garrett AiResearch	?	?
Intel 4004 (4-bit, 16-pin)	2,250	1971	Intel	10,000 nm	12 mm^2
TMX 1795 (?-bit, 24-pin)	3,078[26]	1971	Texas Instruments	?	30 mm^2
Intel 8008 (8-bit, 18-pin)	3,500	1972	Intel	10,000 nm	14 mm^2
NEC μCOM-4 (4-bit, 42-pin)	2,500[27][28]	1973	NEC	7,500 nm[29]	?
Toshiba TLCS-12 (12-bit)	11,000+[30]	1973	Toshiba	6,000 nm	32 mm^2
Intel 4040 (4-bit, 16-pin)	3,000	1974	Intel	10,000 nm	12 mm^2
Motorola 6800 (8-bit, 40-pin)	4,100	1974	Motorola	6,000 nm	16 mm^2
Intel 8080 (8-bit, 40-pin)	6,000	1974	Intel	6,000 nm	20 mm^2
TMS 1000 (4-bit, 28-pin)	8,000	1974[31]	Texas Instruments	8,000 nm	11 mm^2
MOS Technology 6502 (8-bit, 40-pin)	4,528[b][32]	1975	MOS Technology	8,000 nm	21 mm^2
Intersil IM6100 (12-bit, 40-pin; clone of PDP-8)	4,000	1975	Intersil	?	?
CDP 1801 (8-bit, 2-chip, 40-pin)	5,000	1975	RCA	?	?
RCA 1802 (8-bit, 40-pin)	5,000	1976	RCA	5,000 nm	27 mm^2
Zilog Z80 (8-bit, 4-bit ALU, 40-pin)	8,500[c]	1976	Zilog	4,000 nm	18 mm^2
Intel 8085 (8-bit, 40-pin)	6,500	1976	Intel	3,000 nm	20 mm^2
TMS9900 (16-bit)	8,000	1976	Texas Instruments	?	?

Today!

Processors

Tegra Xavier SoC (64/32-bit)	9,000,000,000[127]	2018	Nvidia	12 nm	350 mm^2
AMD Ryzen 7 3700X (64-bit, SIMD, caches, I/O die)	5,990,000,000[128][d]	2019	AMD	7 & 12 nm (TSMC)	199 (74+125) mm^2
HiSilicon Kirin 990 4G	8,000,000,000[129]	2019	Huawei	7 nm	90.00 mm^2
Apple A13 (hexa-core 64-bit ARM64 "mobile SoC", SIMD, caches)	8,500,000,000[130][131]	2019	Apple	7 nm	98.48 mm^2
AMD Ryzen 9 3900X (64-bit, SIMD, caches, I/O die)	9,890,000,000[1][2]	2019	AMD	7 & 12 nm (TSMC)	273 mm^2
HiSilicon Kirin 990 5G	10,300,000,000[132]	2019	Huawei	7 nm	113.31 mm^2
AWS Graviton2 (64-bit, 64-core ARM-based, SIMD, caches)[133][134]	30,000,000,000	2019	Amazon	7 nm	?
AMD Epyc Rome (64-bit, SIMD, caches)	39,540,000,000[1][2]	2019	AMD	7 & 12 nm (TSMC)	1008 mm^2
TI Jacinto TDA4VM (ARM A72, DSP, SRAM)	3,500,000,000 [135]	2020	Texas Instruments	16 nm	
Apple A14 Bionic (hexa-core 64-bit ARM64 "mobile SoC", SIMD, caches)	11,800,000,000[136]	2020	Apple	5 nm	88 mm^2
Apple M1 (octa-core 64-bit ARM64 SoC, SIMD, caches)	16,000,000,000[137]	2020	Apple	5 nm	119 mm^2
HiSilicon Kirin 9000	15,300,000,000[138][139]	2020	Huawei	5 nm	114 mm^2

FPGA Trends

Today!

High-end FPGAs are quite expensive

FPGA Trends

Today!

FPGA	MOS transistor count	Date of introduction	Designer	Manufacturer	MOS process	Area	Ref
Virtex	70,000,000	1997	Xilinx				
Virtex-E	200,000,000	1998	Xilinx				
Virtex-II	350,000,000	2000	Xilinx		130 nm		
Virtex-II PRO	430,000,000	2002	Xilinx				
Virtex-4	1,000,000,000	2004	Xilinx		90 nm		
Virtex-5	1,100,000,000	2006	Xilinx	TSMC	65 nm		[195]
Stratix IV	2,500,000,000	2008	Altera	TSMC	40 nm		[196]
Stratix V	3,800,000,000	2011	Altera	TSMC	28 nm		[197]
Arria 10	5,300,000,000	2014	Altera	TSMC	20 nm		[198]
Virtex-7 2000T	6,800,000,000	2011	Xilinx	TSMC	28 nm		[199]
Stratix 10 SX 2800	17,000,000,000	TBD	Intel	Intel	14 nm	560 mm^2	[200][201]
Virtex-Ultrascale VU440	20,000,000,000	Q1 2015	Xilinx	TSMC	20 nm		[202][203]
Virtex-Ultrascale+ VU19P	35,000,000,000	2020	Xilinx	TSMC	16 nm	900 mm^2 [e]	[204][205][206]
Versal VC1902	37,000,000,000	2H 2019	Xilinx	TSMC	7 nm		[207][208][209]
Stratix 10 GX 10M	43,300,000,000	Q4 2019	Intel	Intel	14 nm	1400 mm^2 [e]	[210][211]
Versal VP1802	92,000,000,000	2021 ?[f]	Xilinx	TSMC	7 nm	?	[212][213]

Memory Trends

?	16 Mb	SRAM (CMOS)	100,663,296	1992	Fujitsu, NEC	400 nm	?	[234]
	256 Mb	DRAM (CMOS)	268,435,456	1993	Hitachi, NEC	250 nm		
	1 Gb	DRAM	1,073,741,824	January 9, 1995	NEC	250 nm	?	[240][241]
					Hitachi	160 nm	?	
		SDRAM	1,073,741,824	1996	Mitsubishi	150 nm	?	[234]
		SDRAM (SOI)	1,073,741,824	1997	Hyundai	?	?	[242]
	4 Gb	DRAM (4-bit)	1,073,741,824	1997	NEC	150 nm	?	[234]
		DRAM	4,294,967,296	1998	Hyundai	?	?	[242]
	8 Gb	SDRAM (DDR3)	8,589,934,592	April 2008	Samsung	50 nm	?	[243]
	16 Gb	SDRAM (DDR3)	17,179,869,184	2008				
	32 Gb	SDRAM (HBM2)	34,359,738,368	2016	Samsung	20 nm	?	[244]
	64 Gb	SDRAM (HBM2)	68,719,476,736	2017				
	128 Gb	SDRAM (DDR4)	137,438,953,472	2018	Samsung	10 nm	?	[245]

Memory Trends

?	1 Gb	2-bit NAND	536,870,912	2001	Samsung	?	?	[234]
					Toshiba, SanDisk	160 nm	?	[251]
	2 Gb	NAND	2,147,483,648	2002	Samsung, Toshiba	?	?	[252][253]
	8 Gb	NAND	8,589,934,592	2004	Samsung	60 nm	?	[252]
	16 Gb	NAND	17,179,869,184	2005	Samsung	50 nm	?	[254]
	32 Gb	NAND	34,359,738,368	2006	Samsung	40 nm		
THGAM	128 Gb	Stacked NAND	128,000,000,000	April 2007	Toshiba	56 nm	252 mm^2	[255]
THGBM	256 Gb	Stacked NAND	256,000,000,000	2008	Toshiba	43 nm	353 mm^2	[256]
THGBM2	1 Tb	Stacked 4-bit NAND	256,000,000,000	2010	Toshiba	32 nm	374 mm^2	[257]
KLMCG8GE4A	512 Gb	Stacked 2-bit NAND	256,000,000,000	2011	Samsung	?	192 mm^2	[258]
KLUFG8R1EM	4 Tb	Stacked 3-bit V-NAND	1,365,333,333,504	2017	Samsung	?	150 mm^2	[259]
eUFS (1 TB)	8 Tb	Stacked 4-bit V-NAND	2,048,000,000,000	2019	Samsung	?	150 mm^2	[4][260]

FPGA Trends

FPGA	MOS transistor count	Date of introduction	Designer	Manufacturer	MOS process	Area	Ref
Virtex	70,000,000	1997	Xilinx				
Virtex-E	200,000,000	1998	Xilinx				
Virtex-II	350,000,000	2000	Xilinx		130 nm		
Virtex-II PRO	430,000,000	2002	Xilinx				
Virtex-4	1,000,000,000	2004	Xilinx		90 nm		
Virtex-5	1,100,000,000	2006	Xilinx	TSMC	65 nm		[195]
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Virtex-Ultrascale VU440	20,000,000,000	Q1 2015	Xilinx	TSMC	20 nm		[202][203]
Virtex-Ultrascale+ VU19P	35,000,000,000	2020	Xilinx	TSMC	16 nm	900 mm^2 [e]	[204][205]
Versal VC1902	37,000,000,000	2H 2019	Xilinx	TSMC	7 nm		[207][208]
Stratix 10 GX 10M	43,300,000,000	Q4 2019	Intel	Intel	14 nm	1400 mm^2 [e]	[210][211]
Versal VP1802	92,000,000,000	2021 ?[f]	Xilinx	TSMC	7 nm	?	[212][213]

Special Purpose Systems

Device type	Device name	Transistor count	Date of introduction	Designer(s)	Manufacturer(s)	MOS process	Area	Ref
Deep learning engine / IPU[g]	Colossus GC2	23,600,000,000	2018	Graphcore	TSMC	16 nm	~800 mm^2	[295][296][297] [*better source needed*]
Deep learning engine / IPU	Wafer Scale Engine	1,200,000,000,000	2019	Cerebras	TSMC	16 nm	46,225 mm^2	[5][6][7][8]
Deep learning engine / IPU	Wafer Scale Engine 2	2,600,000,000,000	2020	Cerebras	TSMC	7 nm	46,225 mm^2	[9][298]

Selected Semiconductor Trends

- AI processors
  - 210 billion transistors, 4nm technology,16cm^2 die area
- Microprocessors
  - now 5 nm with over 40 Billion transistors on a chip
- DRAMS
  - now 128G bits on a chip in a 10nm process which requires somewhere around 140 Billion transistors
- FPGA
  - over 90 Billion transistors at 7nm technology, growing larger

Device count on a chip has been increasing rapidly with time, device size has been decreasing rapidly with time and speed/performance has been rapidly increasing

Moore’s Law

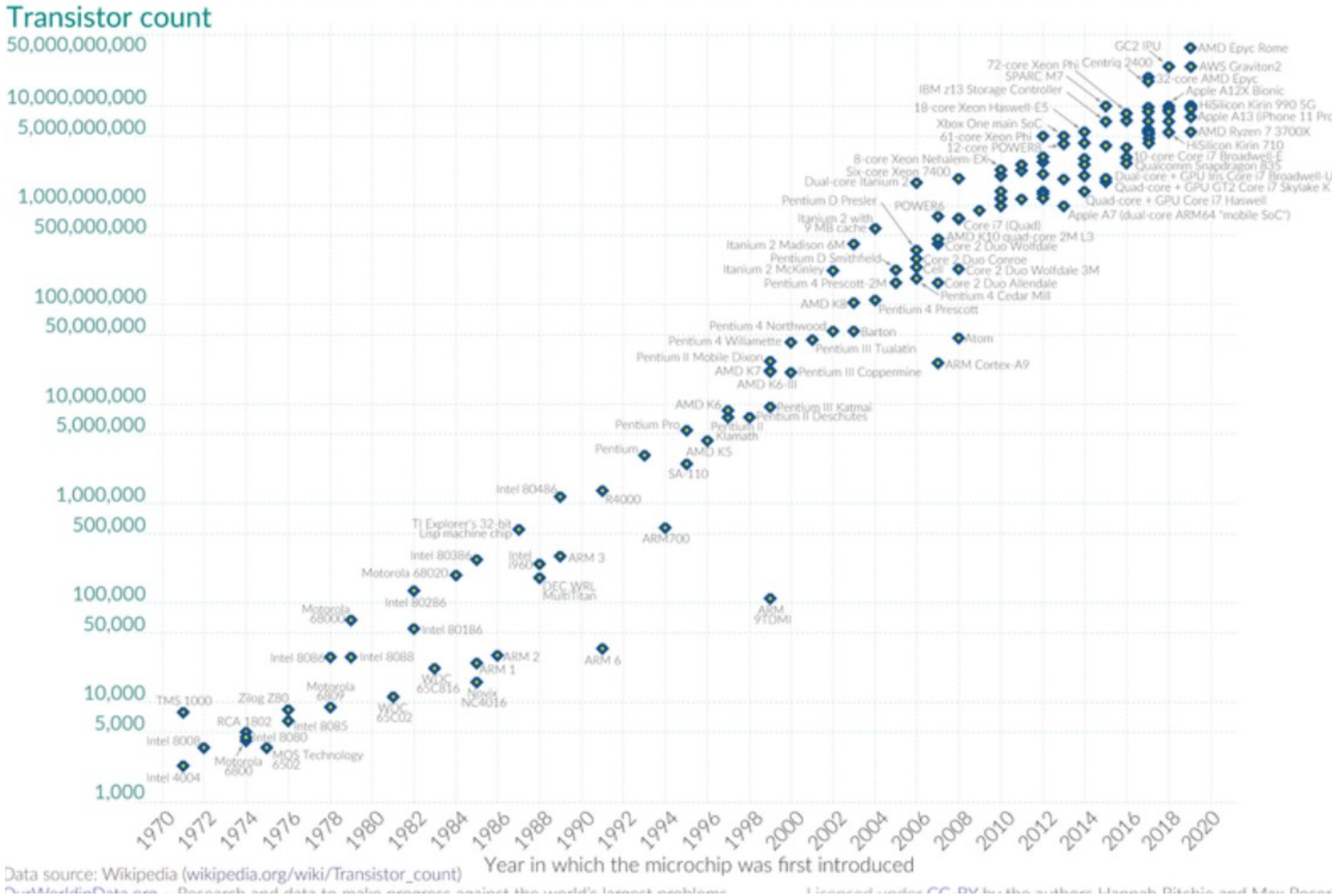
From Webopedia (Aug 2016)

The observation made in 1965 by Gordon Moore, co-founder of Intel, that the number of transistors per square inch on integrated circuits had doubled every year since the integrated circuit was invented. Moore predicted that this trend would continue for the foreseeable future. In subsequent years, the pace slowed down a bit, but data density has doubled approximately every 18 months, and this is the current definition of Moore's Law, which Moore himself has blessed. Most experts, including Moore himself, expect Moore's Law to hold for at least another two decades.

Moore's Law: The number of transistors on microchips doubles every two years

Our World in Data

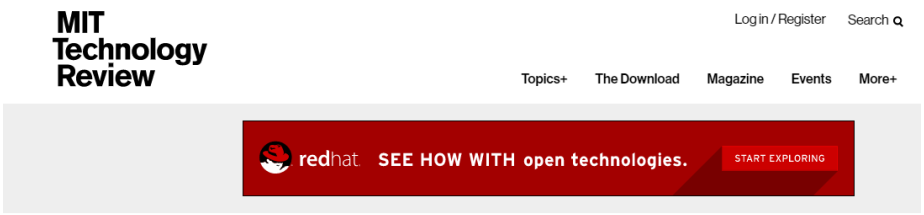
Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important for other aspects of technological progress in computing – such as processing speed or the price of computers.

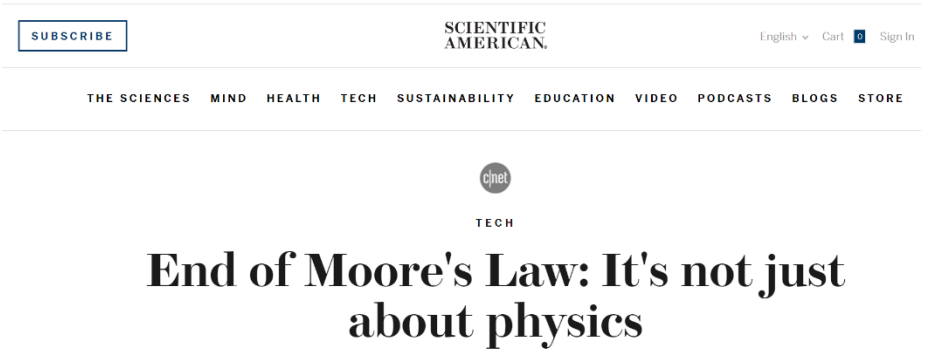


Data source: Wikipedia (wikipedia.org/wiki/Transistor_count)

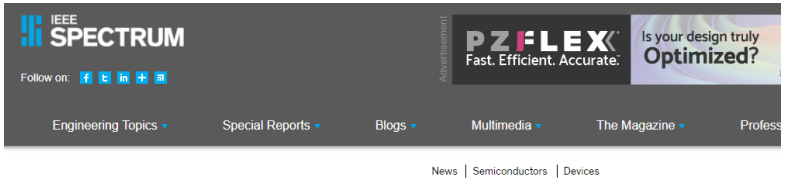
Aug 25, 2021

More on Moore's Law





Moore's Law's End Reboots Industry | EE Times
www.eetimes.com/document.asp?doc_id=1331941
Jun 26, 2017 - The expected death of **Moore's Law** will transform the ... four years, so were reaching the **end** of semiconductor technology as we know it," said ...



Moore's Law Running Out of Room, Tech Looks for a Successor - The ...
https://www.nytimes.com/.../moores-law-running-out-of-room-tech-looks-for-a-successo...
May 4, 2016 - "The **end** of **Moore's Law** is what led to this," said Thomas M. Conte, a Georgia Institute of Technology computer scientist and co-chairman of ...

Moore's Law

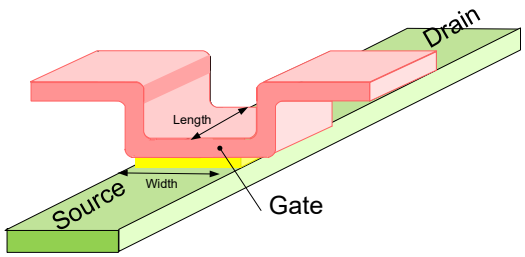
(from Wikipedia)

Moore's law is the empirical observation that the complexity of integrated circuits, with respect to minimum component cost, doubles every 24 months[1]. It is attributed to Gordon E. Moore[2], a co-founder of Intel.

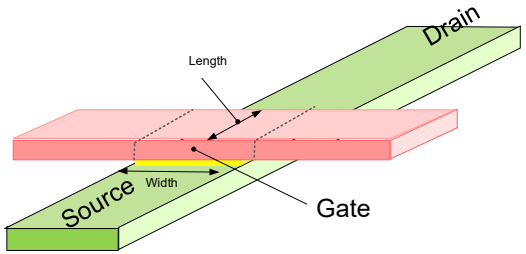
- Observation, not a physical law
- Often misinterpreted or generalized
- Many say it has been dead for several years
- Many say it will continue for a long while
- Not intended to be a long-term prophecy about trends in the semiconductor field
- Something a reporter can always comment about when they have nothing to say!

Device scaling, device count, circuit complexity, device cost, … in leading-edge processes will continue to dramatically improve (probably nearly geometrically with a time constant of around 2 years) for the foreseeable future !!

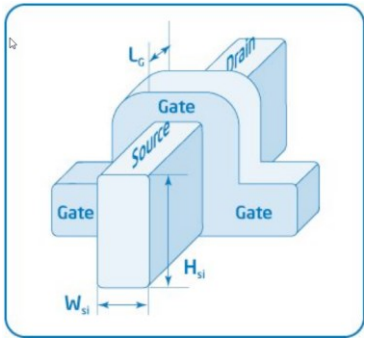
Field Effect Transistors



Planar
MOSFET
(LOCOS)



Planar
MOSFET
(STI)

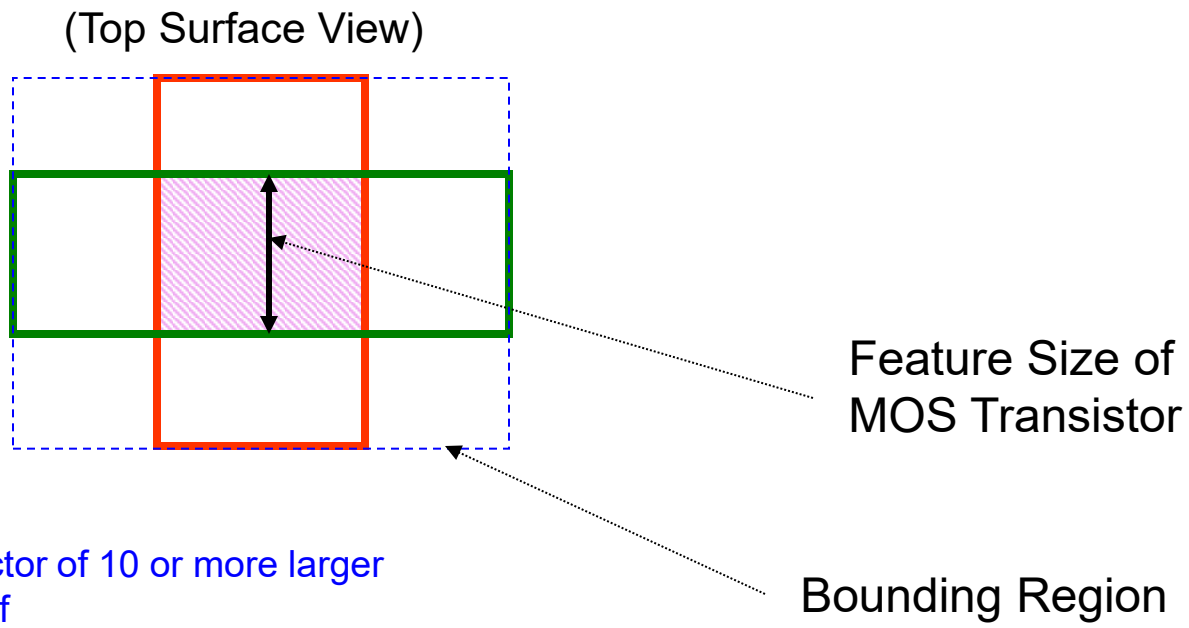


FinFET
Tri-Gate

Dielectric not shown

Feature Size

The feature size of a process generally corresponds to the minimum lateral dimensions of the transistors that can be fabricated in the process



- Bounding region often a factor of 10 or more larger than area of transistor itself
- This along with interconnect requirements and sizing requirements throughout the circuit create an area overhead factor of 10x to 100x

Challenges

- Managing increasing device count
- Short lead time from conception to marketplace
- Process technology advances
- Device performance degradation
- Increasing variability
- Increasing pressure for cost reduction
- Power dissipation

Future Trends and Opportunities

- Is there an end in sight?

No ! But the direction the industry will follow is not yet known but the role semiconductor technology plays on society will increase dramatically!

- Will engineers trained in this field become obsolete at mid-career ?

No ! Engineers trained in this field will naturally evolve to support the microelectronics technology of the future. Integrated Circuit designers are now being trained to efficiently manage enormous levels of complexity and any evolutionary technology will result in even larger and more complexity systems with similar and expanded skills being required by the engineering community with the major changes occurring only in the details.

Future Trends and Opportunities

- Will engineers trained in this field be doing things the same way as they are now at mid-career?

No ! There have been substantive changes in approaches every few years since 1965 and those changes will continue. Continuing education to track evolutionary and revolutionary changes in the field will be essential to remain productive in the field.

- What changes can we expect to see beyond the continued geometric growth in complexity (capability) ?

That will be determined by the creativity and marketing skills of those who become immersed in the technology. New “Gordon Moores”, “Bill Gates” and “Jim Dells” will evolve.

Creation of Integrated Circuits

Most integrated circuits are comprised of transistors along with a small number of passive components and maybe a few diodes

This course will focus on understanding how transistors operate and on how they can be interconnected and possibly combined with a small number of passive components to form useful integrated circuits

Selected Semiconductror Company Profiles

(with Iowa ties)

Texas Instruments:

- World's largest producer of analog semiconductors at $15.4B, over 100% larger than closest competitor
- Ranks 1st in DSP
- Ranks 9th in World in semiconductor sales

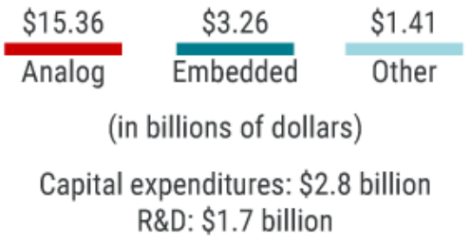
Number of employees: 31,000

2022 sales: $20B

2022 income: $8.7B
(after taxes)

Average annual sales/employee: $645K

Average annual earnings/employee: $280K



~ 14,000 in the Americas

~ 17,000 in Asia-Pacific

~ 2,000 in Europe

Jerry Junkins

Past CEO of TI
ISU EE Class of '59

(data from WWW)

Selected Semiconductror Company Profiles

(with Iowa ties)

Intel:

World's largest producer of semiconductors

Cofounders: Robert Noyce and Gordon Moore

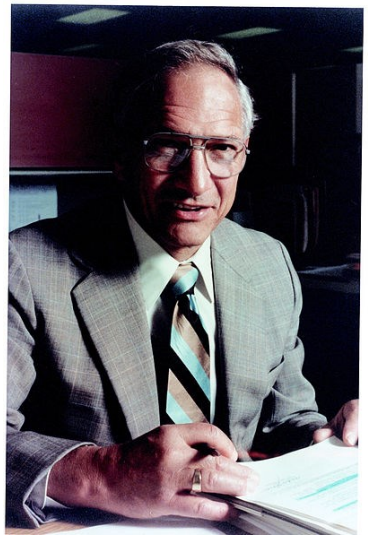
Number of employees (2022) : 132,000

2022 sales: $63B down 20%

2022 income: $8B down 60%

Average annual sales/employee: $480K

Average annual earnings/employee: $60K



Robert Noyce

BA Grinnell 1949

Noyce is also the co-inventor of the integrated circuit !

Selected Semiconductror Company Profiles

(with Iowa ties)

Marvell:

Cofounders: Sehat Sutardja (CEO), Welli Dai and Pantas Sutardja

Number of employees: 7400 (Jan 2023)

2022 sales: $5.9B

2022 income: $3.0B

Average annual sales/employee: $790K

Average annual earnings/employee: $405K

Fabless Semiconductor Company

Sehat Sutardja

BSEE ISU
(approx 1985)

Selected Semiconductror Company Profiles

(with Iowa ties)

Maxim: Founded in April 1983, profitable every year since 1987

Tunc Doluca joined Maxim in October 1984, appointed President and CEO in 2007

Number of employees: 7100

2021 sales: $2.6B

2021 income: $827M

Average annual sales/employee: $370K

Average annual earnings/employee: $116K

Tunc Doluca

BSEE IASTATE

(1979)

(now a part of Analog Devices)

Considerable Cash Flow Inherent in the Semiconductor Industry

Essentially All Activities Driven by Economic Considerations

- Many Designs Cost Tens of Millions of Dollars
- Mask Set and Production of New Circuit Approaching $2 Million
- New Foundries Costs Approaching $10 Billion (few players in World can compete)
- Many Companies Now Contract Fabrication (Fabless Semiconductor Companies)
- Time to Market is Usually Critical
- Single Design Error Often Causes Months of Delay and Requires New Mask Set
- Potential Rewards in Semiconductor Industry are Very High

Will emphasize economic considerations throughout this course

Understanding of the Big Picture is Critical

Solving Design Problems can be Challenging

Be sure to solve the right problem !

How can complex circuits with a very large number of transistors be efficiently designed with low probability of error?

- Many designers often work on a single design
- Single error in reasoning, in circuit design, or in implementing circuit on silicon generally results in failure
- Design costs and fabrication costs for test circuits are very high
  - Design costs for even rather routine circuits often a few million dollars and some much more
  - Masks and processing for state of the art processes often between $1M and $2M
- Although much re-use is common on many designs, considerable new circuits that have never been designed or tested are often required
- Time to market critical – missing a deadline by even a week or two may kill the market potential

Single Errors Usually Cause Circuit Failure

- How may components were typical of lab experiments in EE 201 and EE 230?
- Has anyone ever made an error in the laboratory of these courses ? (wrong circuit, incomplete understanding, wrong wiring, wrong component values, imprecise communication, frustration …..)
- How many errors are made in a typical laboratory experiment in these courses?
- How many errors per hour might have occurred?

Single Errors Usually Cause Circuit Failure

Consider an extremely complicated circuit

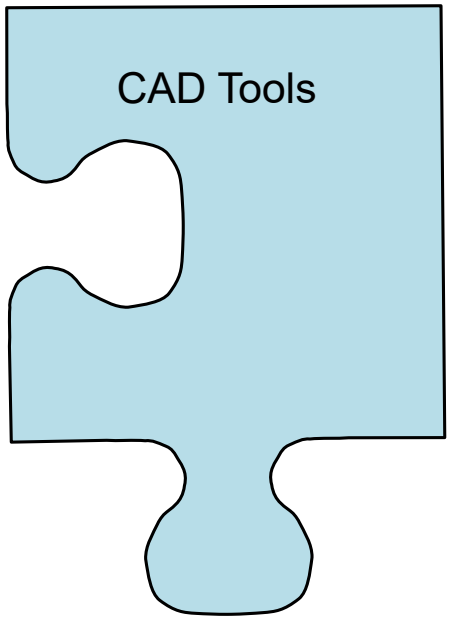
- with requirements to do things that have never been done before
- with devices that are not completely understood
- that requires several billion transistors
- that requires 200 or more engineers working on a project full-time for 3 years
- with a company investment of many million dollars
- with an expectation that nobody makes a single error

Is this a challenging problem for all involved?

How can complex circuits with a very large number of transistors be efficiently designed with low probability of error?

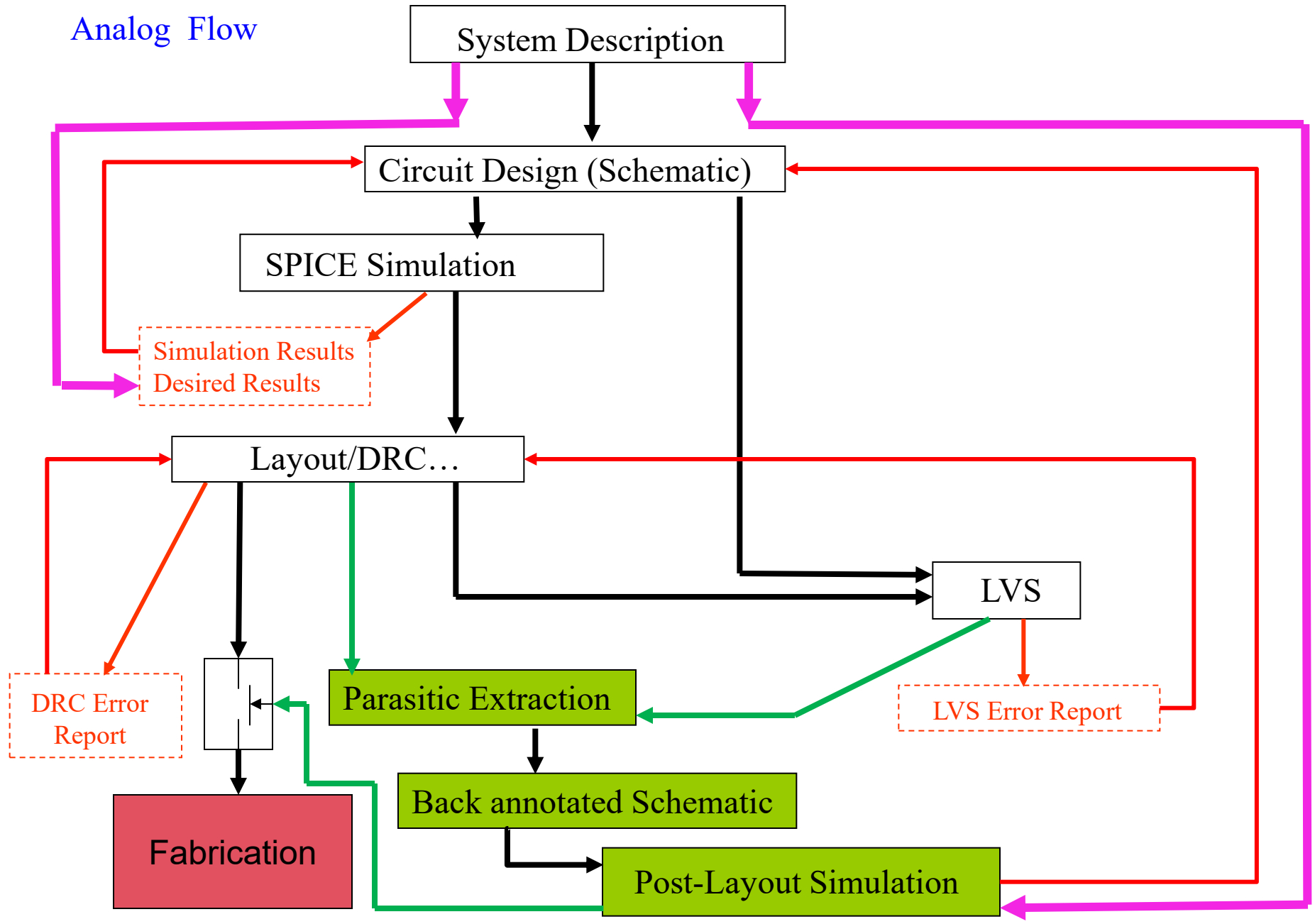
- CAD tools and CAD-tool environment critical for success today
- Small number of VLSI CAD toolset vendors
- CAD toolset **helps the engineer** and it is highly unlikely the CAD tools will replace the design engineer
- CAD toolset will replace some of the tasks a design engineer does so engineer can address emerging challenges
- An emphasis in this course is placed on using toolset to support the design process

CAD Environment for Integrated Circuit Design

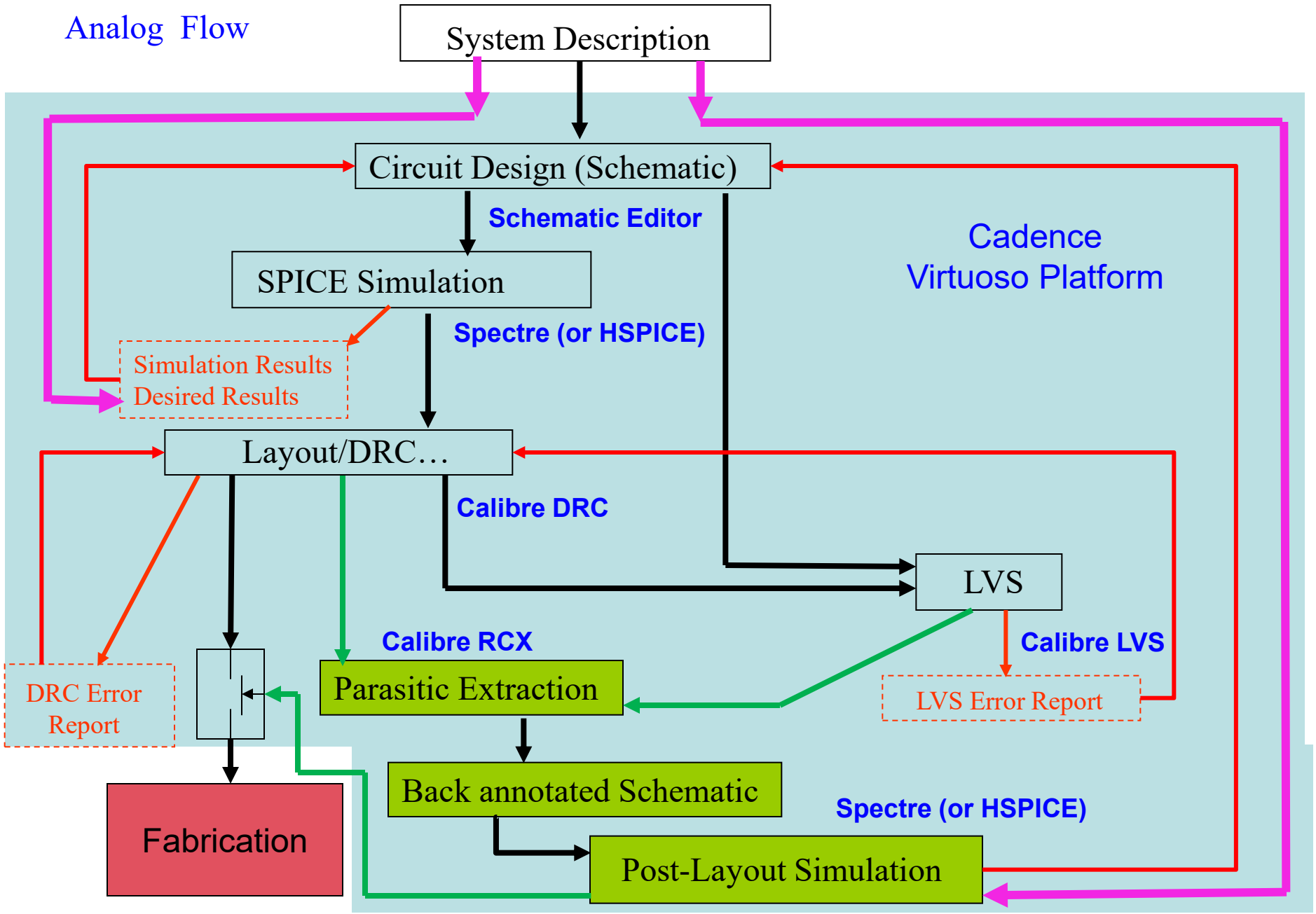


- Typical Tool Flow
  - (See Chapter 14 of Text)
- Laboratory Experiments in Course

VLSI Design Flow Summary

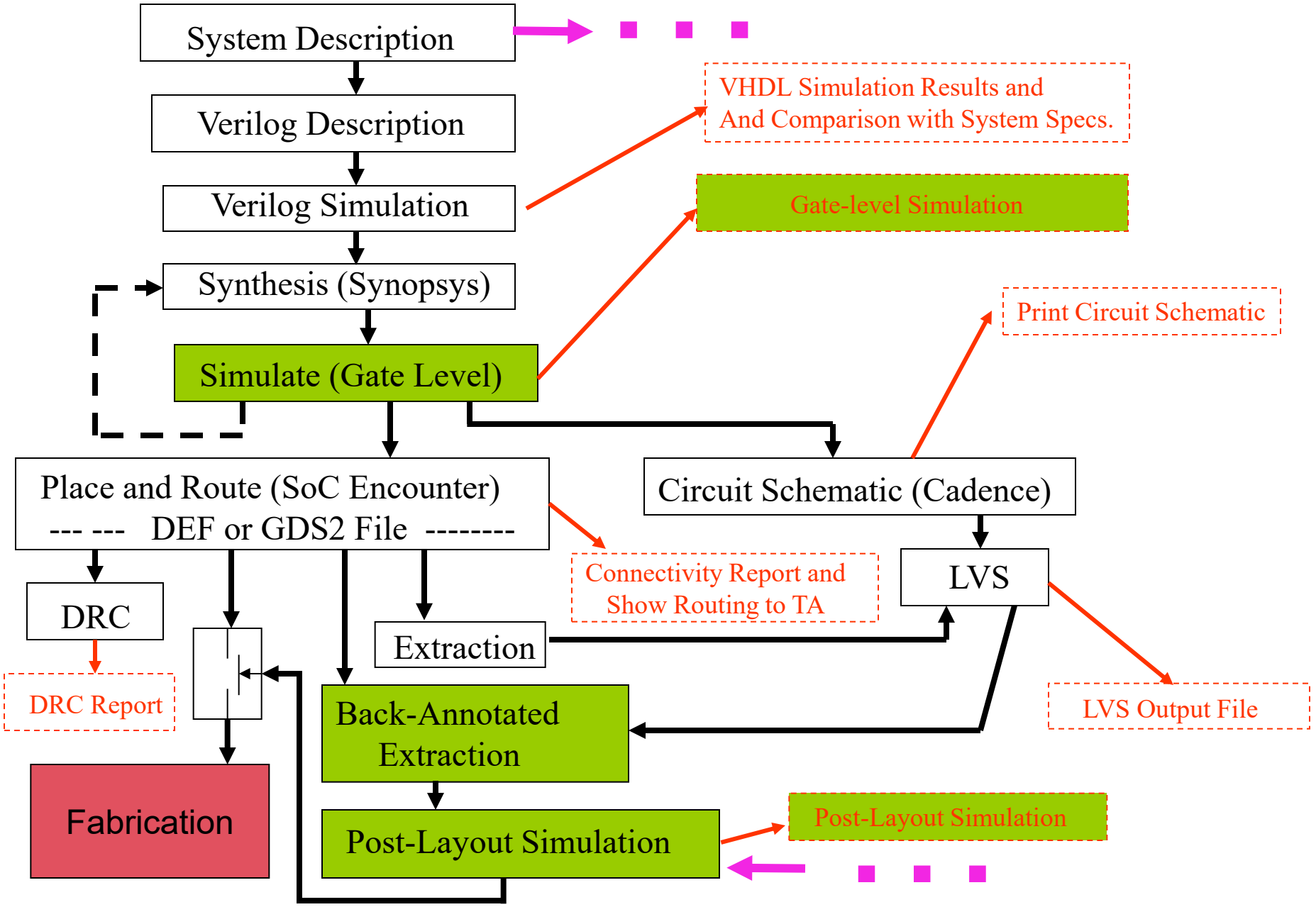


VLSI Design Flow Summary



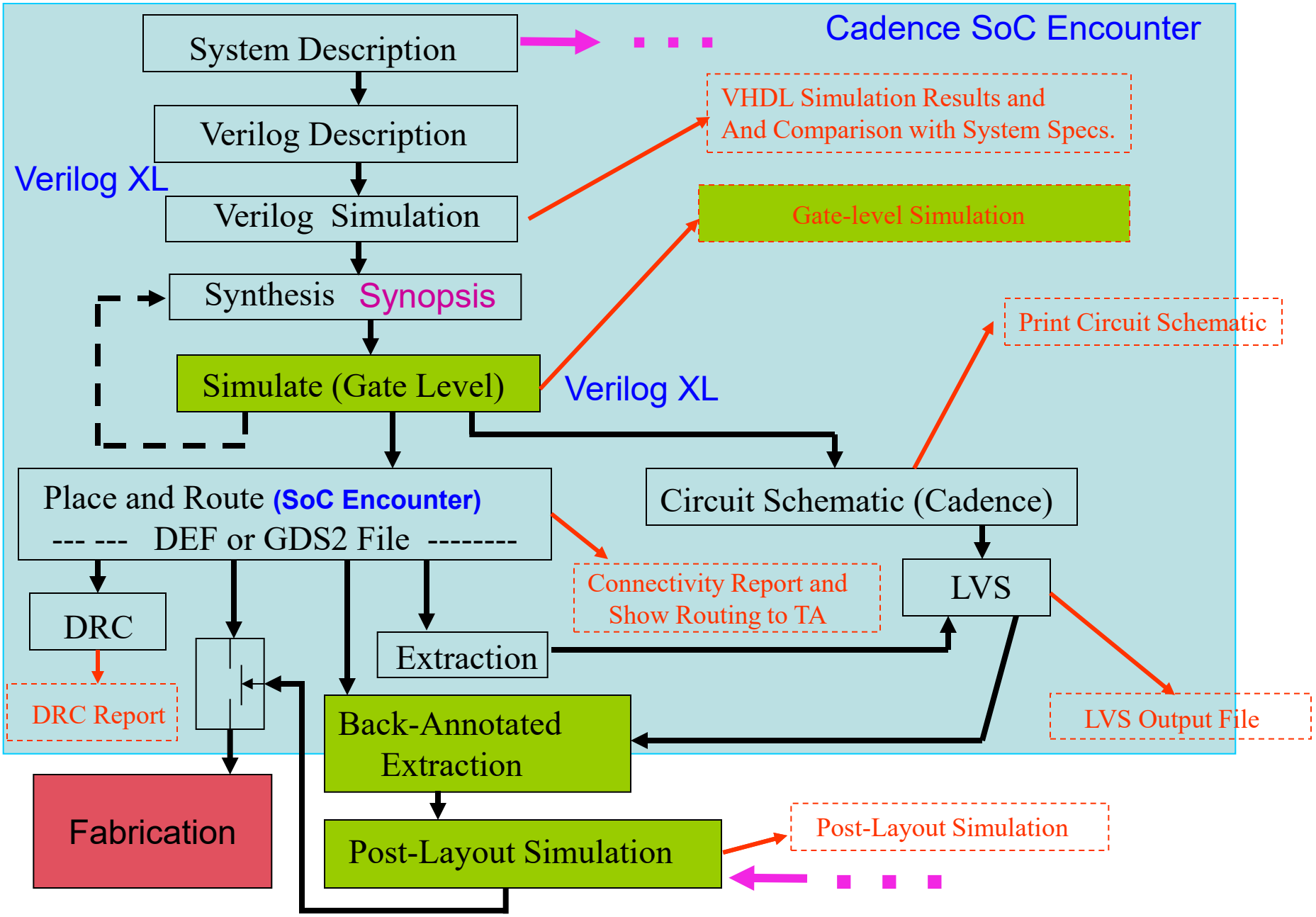
VLSI Design Flow Summary

Digital Flow



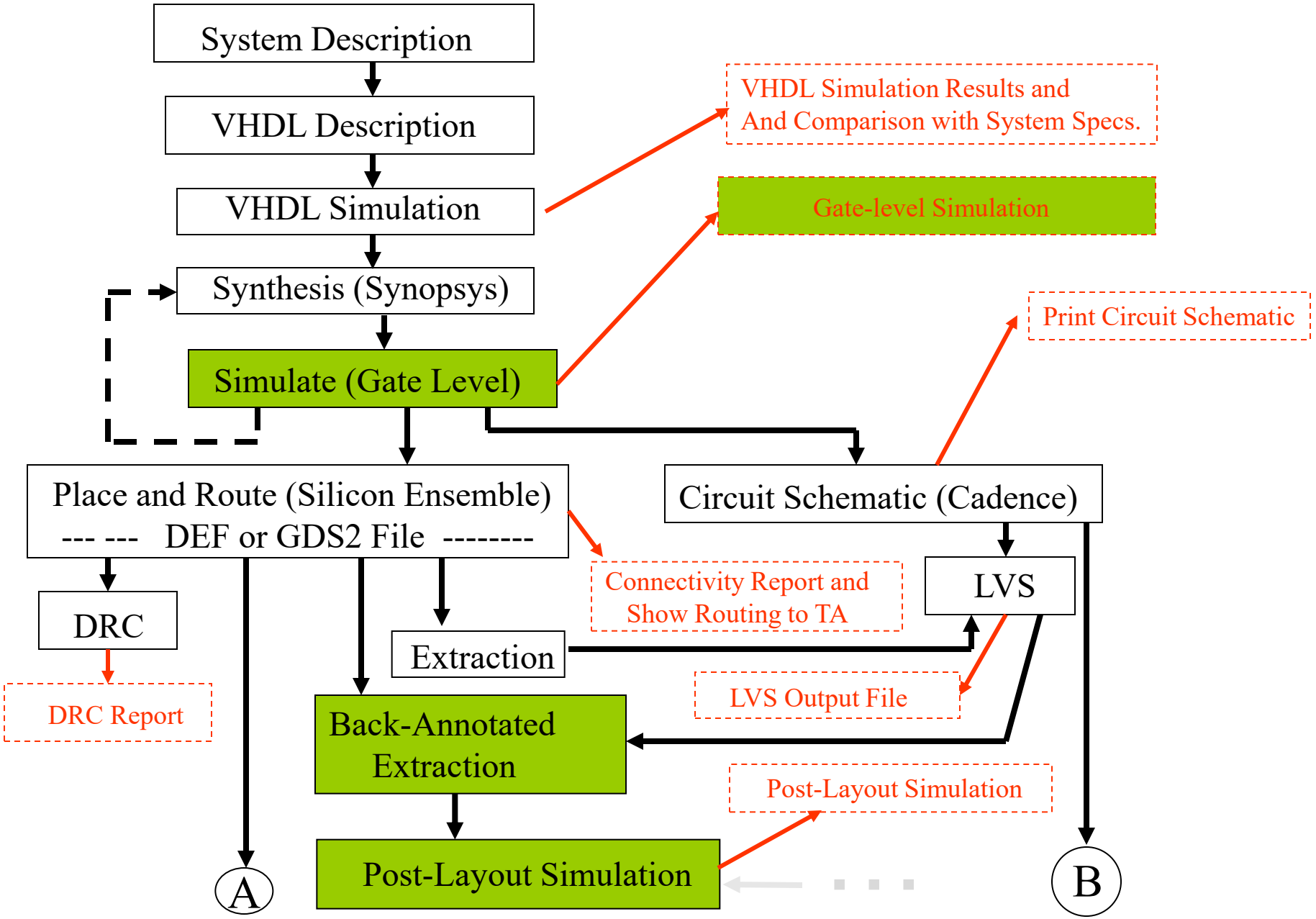
VLSI Design Flow Summary

Digital Flow

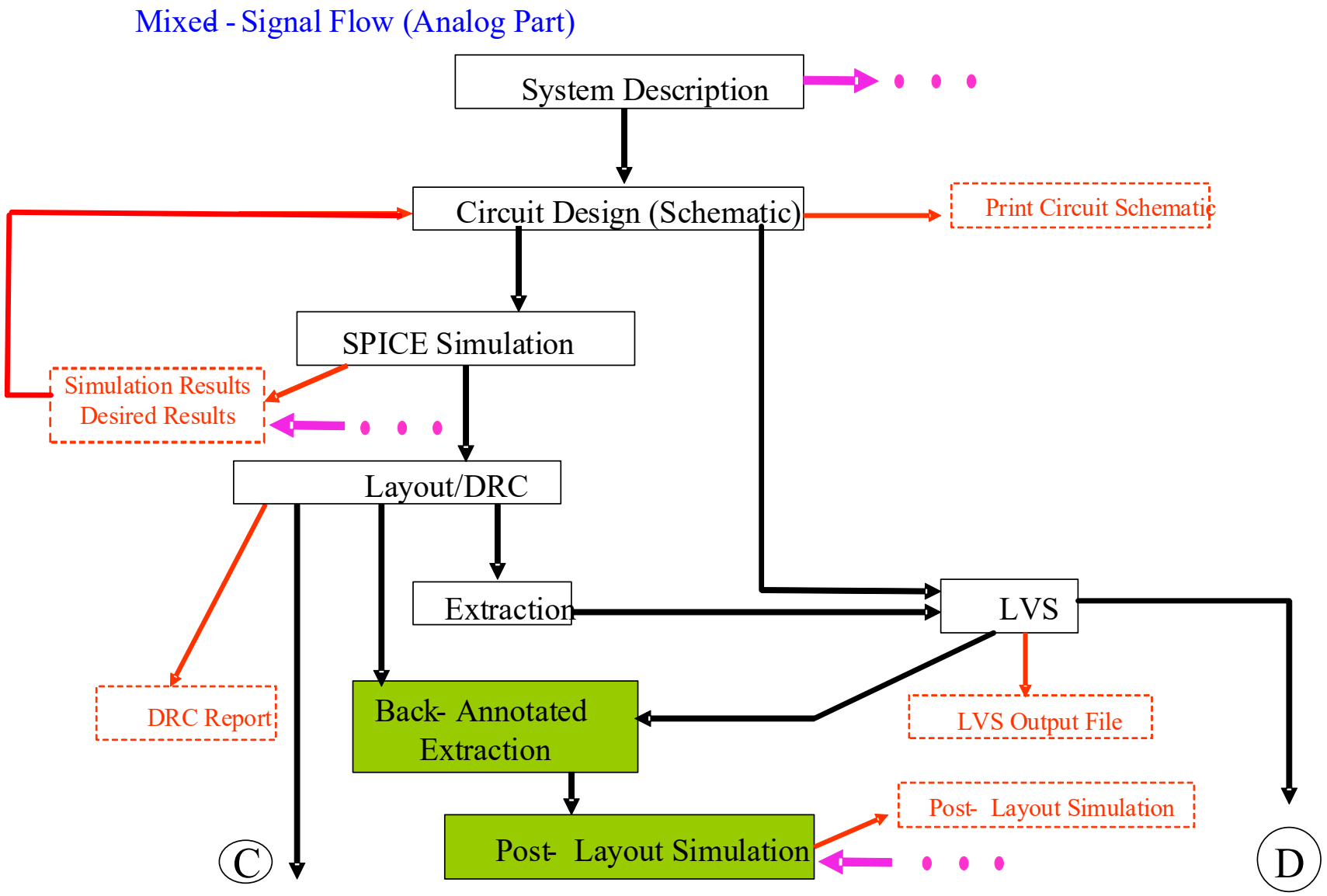


VLSI Design Flow Summary

Mixed Signal Flow (Digital Part)

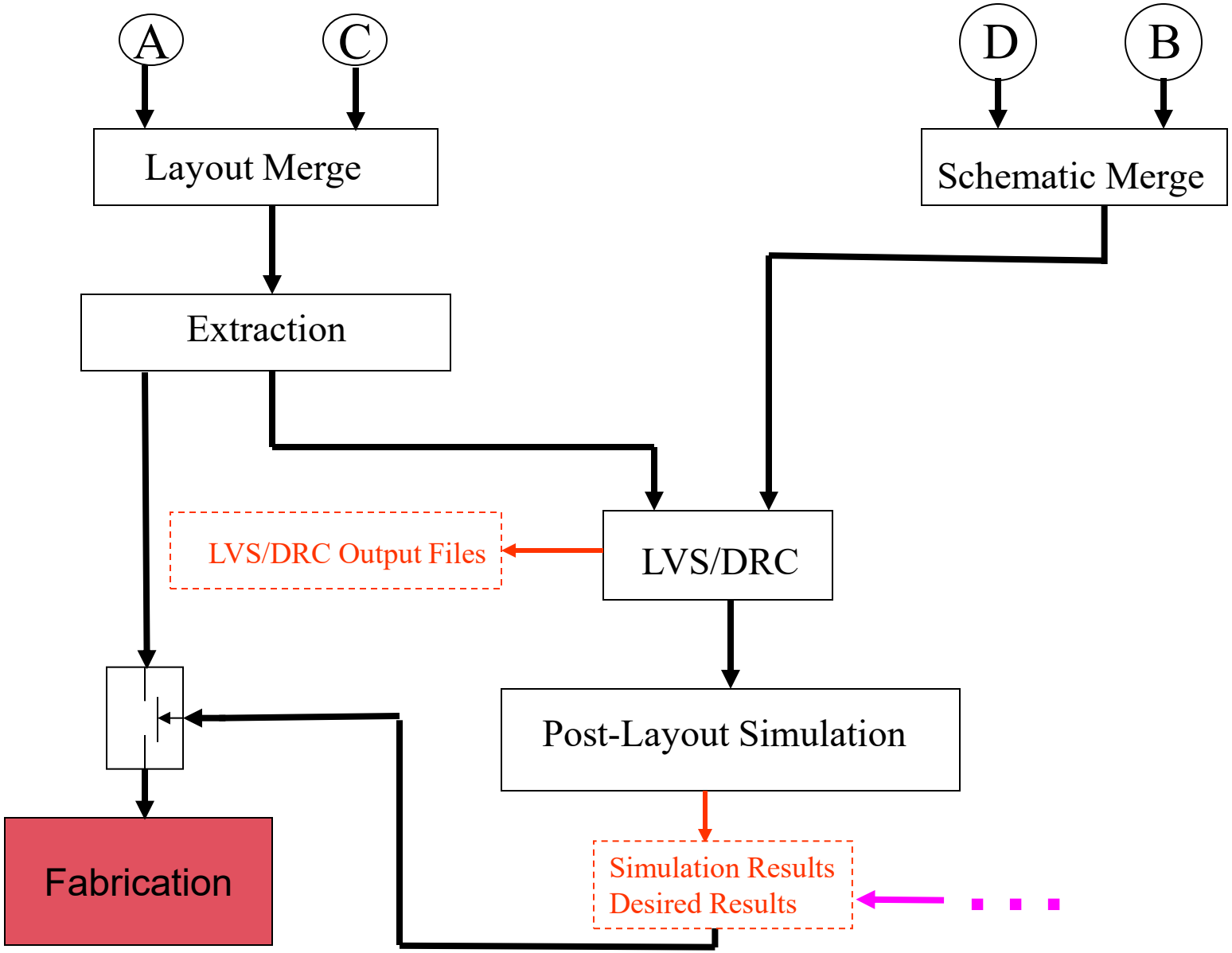


VLSI Design Flow Summary



VLSI Design Flow Summary

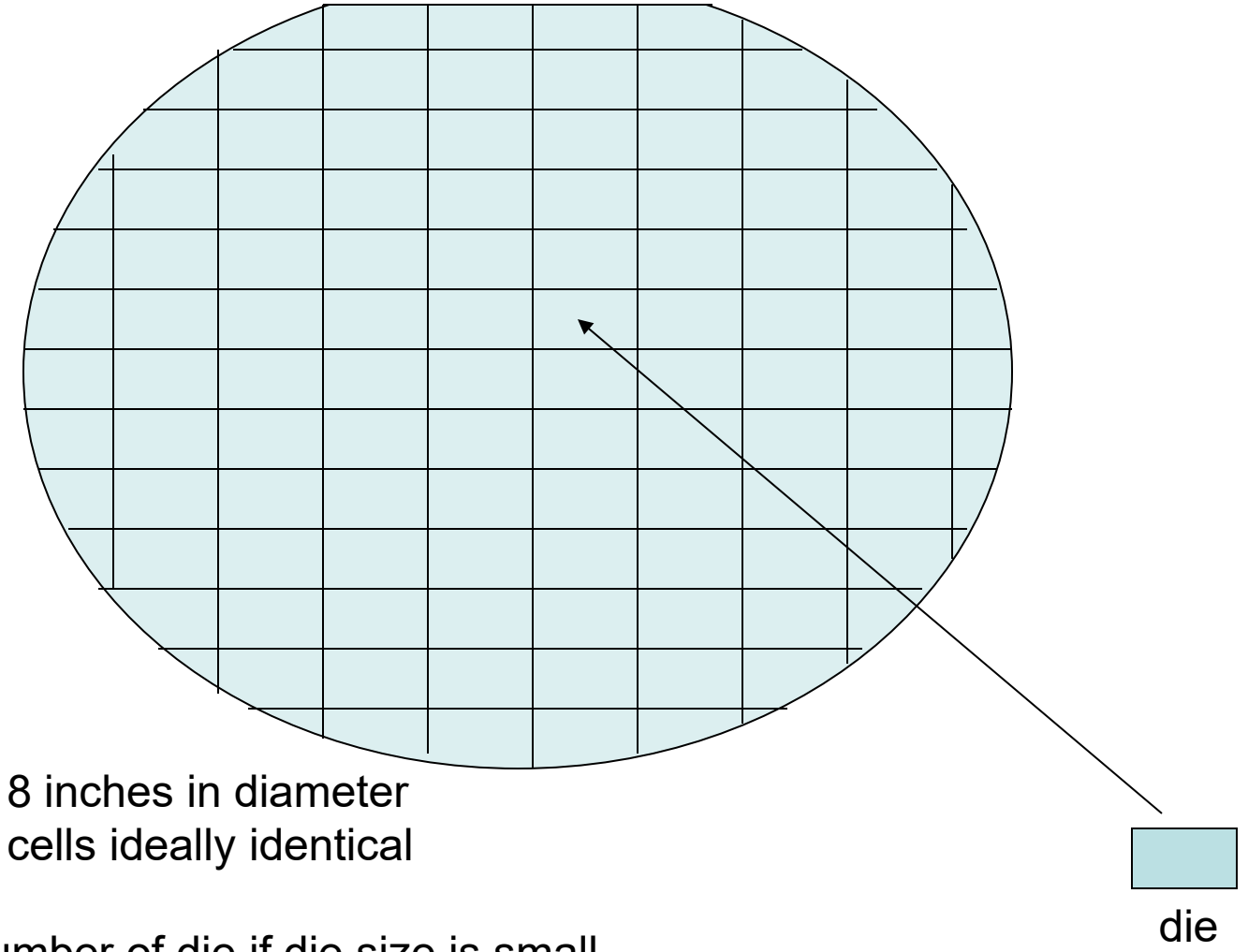
Mixed-Signal Flow (Analog-Digital Merger)



Comments

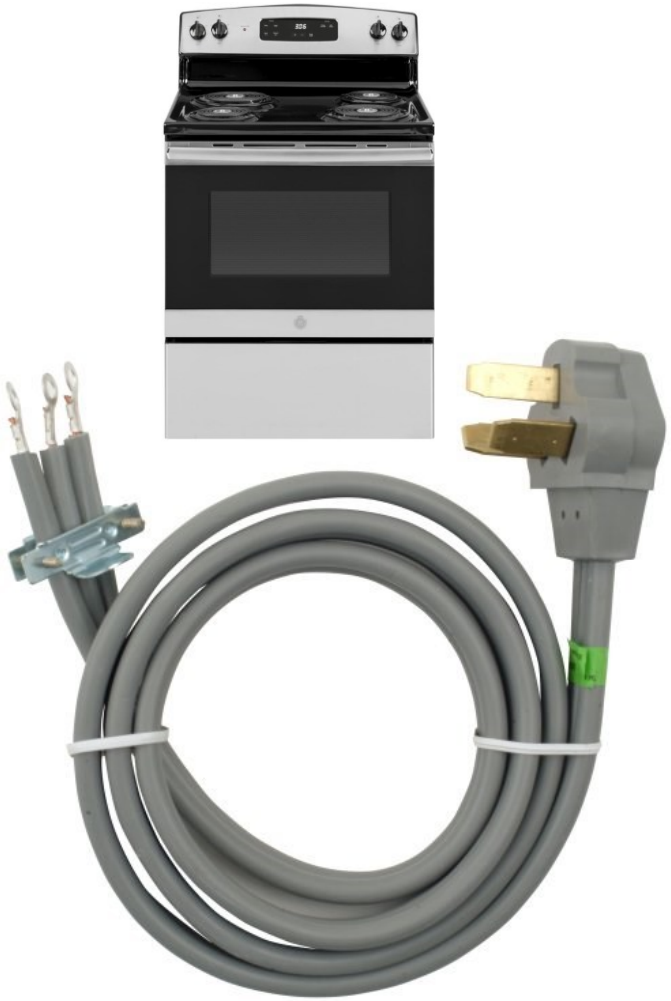
- The Analog Design Flow is often used for small digital blocks or when particular structure or logic styles are used in digital systems
- Variants of these flows are widely used and often personalized by a given company or for specific classes of circuits

Wafer



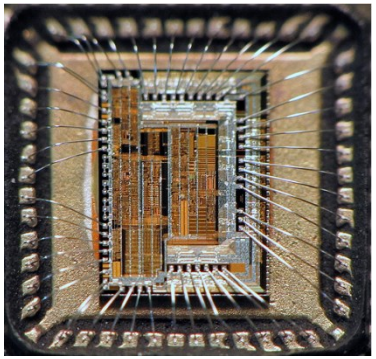
- 6 inches to 18 inches in diameter
- All complete cells ideally identical
- flat edge
- very large number of die if die size is small

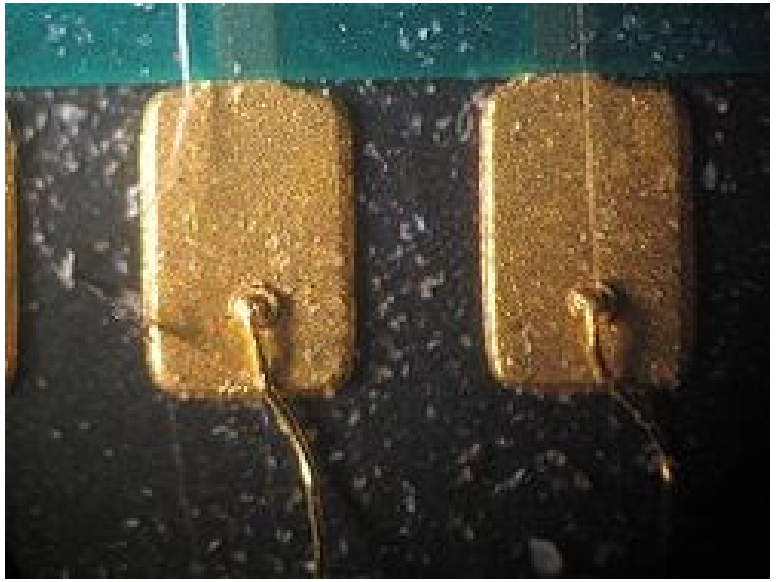
Wire Sizes for Electrical Interconnects



50 A Range Cord

6 ga Wiring 0.162 in diameter





25um Gold Bonding Wire

Stay Safe and Stay Healthy !

End of Lecture 2